IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		TI-37350
	Robert F. Payne, et al.	Art Unit: 2816
Serial No:	10/765,377	Examiner: Thuan Thieu Lam
Filed:	January 27, 2004	Conf. No.: 1598
For:	High Performance Sense Amplifiers	

Amended Appeal Brief Summary of Claimed Subject Matter

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Amended Summary of Claimed Subject Matter in connection with the above-identified application in response to the Notification of Non-Compliant Appeal Brief mailed **August 17, 2007**.

SUMMARY OF CLAIMED SUBJECT MATTER

Specification page 4, line 13 to page 6, line 4, provides a concise explanation of the invention defined in claim 1.

Figure 1 shows a sense amplifier ("SA") in accordance with an exemplary embodiment of the invention. As shown, the SA 10 comprises a regenerative latch 11 coupled to an input differential transistor pair. The regenerative latch comprises N-channel field effect transistors ("nFETs") 36,38 and P-channel field effect transistors ("pFETs") 20-34. The input differential

transistor pair comprises nFET transistors 12 and 14 and receives differential input signals INP and INN. The nFET transistor 16 comprises a clocked current source that alternatively enables and disables the differential transistor pair 12, 14. The R and S signals represent differential output signals from the SA and are generated by the regenerative latch 11 and latched by SR latch 40.

In operation, the SA 10 preferably undergoes a "precharge" phase and an "evaluate" phase as illustrated in Figure 2. When CLOCK is low, the R and S nodes pre-charge to a high state. That is, both R and S are high during the pre-charge phase. During the evaluate phase (clock high), the SA 10 asserts S high and R low when the INN voltage is greater than the INP voltage and asserts R high and S low when INP is greater than INN. The evaluate phase begins with each rising clock edge. A time delay called the "clock-to-Q" delay (CLK2Q) defines the time required by a sense amplifier to resolve the input differential signals (INN and INP) and generate the R and S signals following a rising clock edge.

Referring again to Figure 1, nFET 16 is turned on and off by the CLOCK signal and accordingly causes the input differential transistor pair 12, 14 to turn on and off. During the pre-charge phase (clock low), nFET 16 is off thereby forcing input differential transistor pair 12, 14 to be off. Upon entering the evaluate phase, with the input differential pair 12,14 off, it takes time (i.e., the CLK2Q delay) to discharge node 15, turn the input differential pair 12, 14 back on to conduct current via nFET 16, and begin evaluating the differential input signals INP and INN. The SA 10 preferably includes a leakage device 44 to reduce the CLK2Q time delay. The leakage device 44 preferably comprises a field effect transistor such as an nFET with the source grounded, drain connected to node 15 and gate tied high. Other suitable types of devices or configurations of the transistors may be used in place of an nFET for this purpose. The leakage device 44 functions to maintain the input differential transistor pair 12, 14 in an "on" state even during the pre-charge phase. By keeping the input differential transistor pair on, the transistors 12, 14 can react quicker than would otherwise be possible, thereby reducing the CLK2Q time delay and decreasing the resolution time of the sense amplifier. Further, the leakage device 44 also causes the R and S differential outputs to be biased relative to each other so as to reflect the voltage difference between INP and INN during the pre-charge phase. That is, if INP is greater than INN, even during pre-charge R will be maintained at a higher voltage than S. By

encouraging, during pre-charge, the differential output signals towards their ultimate evaluated voltages, the CLK2Q delay can be further reduced.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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CLAIMS APPENDIX

1. A sense amplifier, comprising:

a regenerative latch;

an input differential pair of transistors coupled to the regenerative latch;

a leakage device coupled to each of the transistors comprising the input differential pair of transistors, said leakage device adapted to maintain the input differential pair of transistors in an on state during a pre-charge phase; and

wherein the regenerative latch comprises a first transistor coupled between the pair of transistors, a second transistor coupled to a first one of the pair of transistors, and a third transistor coupled to a second one of the pair of transistors, wherein the first, second, and third transistors are controlled by a clock signal node.

2. The sense amplifier of claim 1 wherein the leakage device comprises a field effect transistor.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None